In the Claims:

1. (Currently Amended) A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate including at least one interconnect formed on the first semiconductor substrate and also including at least one contact area that is electrically connected to the interconnect and is arranged on a side surface of the first semiconductor substrate; and

a second semiconductor substrate having at least one interconnect formed on the second semiconductor substrate and also including at least one contact area that is electrically connected to the interconnect and is arranged on a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged on the first semiconductor substrate and the first semiconductor substrate is arranged on the mount element such that a first main surface of the second semiconductor substrate rests on the first semiconductor substrate, and a first main surface of the first semiconductor substrate rests on the mount element, and wherein an electrical contact is produced between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate and wherein the first and second semiconductor substrates each comprise an unpackaged semiconductor chip with integrated circuitry disposed therein.

2. (Currently Amended) The semiconductor chip arrangement of claim 1 wherein the first and second semiconductor substrates each have the integrated circuitry disposed in the area of the first main surface, wherein, for both the first and second semiconductor substrates, the integrated circuitry is electrically coupled to the interconnect.

3. (Original) The semiconductor chip arrangement of claim 1 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

4. (Original) The semiconductor chip arrangement of claim 1 wherein the first main surface of the first semiconductor substrate is attached to the mount element.

5. (Original) The semiconductor chip arrangement of claim 1 wherein the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate each extend from the first main surface to a second main surface of the respective semiconductor substrate.

6. (Original) The semiconductor chip arrangement of claim 1 wherein each of the first and second semiconductor substrates includes a dynamic random access memory formed therein.

7. (Currently Amended) A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate arranged over a surface of the mount element, the first semiconductor substrate including at least one interconnect formed thereon, the first semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the first semiconductor substrate;

a second semiconductor substrate arranged over the surface of the mount element alongside the first semiconductor substrate, the second semiconductor substrate including at least one interconnect formed thereon, the second semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side

surface of the second semiconductor substrate, the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate; and

a third semiconductor substrate arranged over the second semiconductor substrate, the third semiconductor substrate including at least one interconnect formed thereon, the third semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the third semiconductor substrate, the third semiconductor substrate arranged so that an electrical contact is produced between the contact area of the third semiconductor substrate and the contact area of the second semiconductor substrate;

wherein the first, second and third semiconductor substrates each comprise unpackaged semiconductor chips with integrated circuitry disposed in the area of a first main surface such that the integrated circuit is electrically coupled to the interconnect, the first main surface being parallel to the surface of the mount element.

8. (Canceled)

9. (Original) The semiconductor chip arrangement of claim 7 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

10. (Original) The semiconductor chip arrangement of claim 7 wherein the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element.

11. (Original) The semiconductor chip arrangement of claim 7 wherein the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrate.

12. (Original) The semiconductor chip arrangement of claim 11 wherein the contact area on the third semiconductor substrate extends to a first main surface on the third semiconductor substrate.

13. (Currently Amended) The semiconductor chip arrangement of claim 7 wherein the integrated circuitry of each of the first, second, and third semiconductor substrates includes a dynamic random access memory ~~formed therein~~.

14–19. (Canceled)

20. (New) A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate arranged over a surface of the mount element, the first semiconductor substrate including at least one interconnect formed thereon, the first semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the first semiconductor substrate; and

a second semiconductor substrate arranged over the surface of the mount element alongside the first semiconductor substrate, the second semiconductor substrate including at least one interconnect formed thereon, the second semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate; and

wherein the first, and second semiconductor substrates each comprise an unpackaged semiconductor substrate having integrated circuitry disposed in the area of a first main surface, the first main surface being parallel to the surface of the mount element.

21. (New) The semiconductor chip arrangement of claim 20, wherein each of the semiconductor substrates the integrated circuitry is electrically coupled to the interconnect.

22. (New) The semiconductor chip arrangement of claim 20 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

23. (New) The semiconductor chip arrangement of claim 20 wherein the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element.

24. (New) The semiconductor chip arrangement of claim 20 wherein the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrates.

25. (New) The semiconductor chip arrangement of claim 20 wherein each of the first and second semiconductor substrates includes a dynamic random access memory formed therein.

26. (New) The semiconductor chip arrangement of claim 1, wherein the second semiconductor substrate is arranged in direct contact with the first semiconductor substrate and the first semiconductor substrate is arranged in direct contact with the mount element.

27. (New) The semiconductor chip arrangement of claim 7, wherein the first semiconductor substrate arranged in direct contact with the surface of the mount element, the second semiconductor substrate arranged in direct contact with the surface of the mount element, and the third semiconductor substrate arranged in direct contact with the second semiconductor substrate.